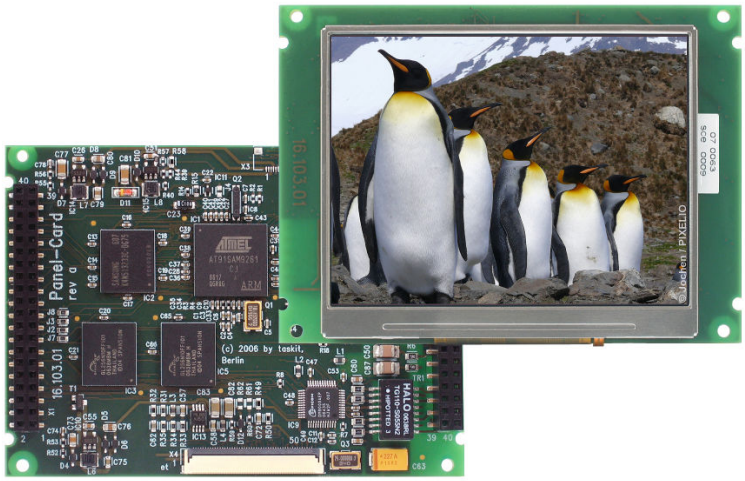

Panel-Card

Technical Reference

Panel-Card: Technical Reference

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1. Introduction

The Panel-Card is intended to be used as a small and medium size "intelligent" display module as well as a universal Linux CPU card. It can be used where restricted energy and space requirements play a role. It comes in different sizes and variations, but the connector keeps the same, likewise the center of the LCD/TFT. Thus one baseboard can carry different Panel-Cards, easily adopting to different needs.

The Panel-Card70 is also available in a rugged aluminium housing as Desk70.

The Panel-Card has all the necessary interfaces to support a huge variety of peripheral devices. Dispensing with a parallel bus keeps the pin count small and makes it possible to use rugged, inexpensive standard connectors.

The ARM architecture as a modern and widely supported processor architecture is currently the platform of choice for medium performance embedded devices. Almost all major processor manufacturers have ARM products in their portfolio.

The availability of the widespread operating system "Linux" for the ARM platform opens access to a broad range of software, including tools, drivers, and software libraries. Programs written for ARM can easily be employed on the PC platform for testing and debugging.

Examples of actual or potential applications are: terminals, measuring and test equipment, data-logging, as well as any simple or more complex control and automation tasks.

2. Scope

This document covers the following Panel-Card's:

- Panel-Card 35 TFT 320x240 transmissive
- Panel-Card 57 TFT 320x240
- Panel-Card 57 TFT 640x480
- Panel-Card 70 TFT 800x480

This document describes the most important hardware features of the Panel-Card. It includes all informations necessary to develop a customer specific hardware for the Panel-Card. The Operating System Linux is described in a further document.

The manual comprises only a brief description of the AT91SAM9261 processor, as this is already described in depth in the manual of the manufacturer Atmel. Descriptions of the ARM core ARM926EJ-S are available from Atmel and also at *http://www.arm.com*. It is much recommended to have a look at these documents for a thorough understanding of the processor and its integrated peripherals.

The datasheet of the Ethernet controller is available at *http://www.davicom.com.tw*.

3. Overview of Technical Characteristics

3.1. CPU

Atmel AT91SAM9261 Embedded Processor featuring an ARM926EJ-S™ ARM® Thumb® Core

- CPU clock 200 MHz
- 16KB Instruction Cache
- 16KB Data Cache
- Memory Management Unit (MMU)
- 3.3V Supply Voltage, 1.2V Core Voltage

3.2. Memory

- 16 or 64 MB NOR flash memory (optional more)
- 32 or 64 MB SDRAM
- 160 KB fast SRAM
- 256 Bytes EEPROM

3.3. Display

- 3.5″ TFT with 320x240 pixels, transmissive
  - 0.219 mm dot pitch
  - Active area 70.08 x 52.56 mm
  - Color depth of 8, 16 or 24 bit per pixel
  - Touchscreen optionally available
- 3.5″ TFT with 240x320 pixels, transflective
  - 0.2235 mm dot pitch
  - Active area 53.64 x 71.52 mm
  - Color depth of 8, 16 or 18 bit per pixel
  - Touchscreen included
- 5.7″ TFT with 320x240 pixels, transmissive
  - 0.36 mm dot pitch

    - Active area 115.2 x 86,4 mm
    - Color depth of 8, 16 or 24 bit per pixel
    - Touchscreen included
- 5.7″ TFT with 640x480 pixels, transmissive
    - 0.18 mm dot pitch
    - Active area 115.2 x 86.4 mm
    - Color depth of 8, 16 or 24 bit per pixel
    - Touchscreen included
- 7.0″ TFT with 800x480 pixels, transmissive
    - 0.1905 mm dot pitch
    - Active area 152.4 x 91.44 mm
    - Color depth of 8, 16 or 18 bit per pixel
    - Touchscreen included

3.4. Interfaces and external signals

- Ethernet 10/100 Mbit MAC
- Dual USB 2.0 Full Speed (12 MBit/s) Hosts
- USB 2.0 Full Speed (12 MBit/s) Device
- Three USARTs
- One UART
- One Synchronous Serial Controller (SSC, I^2S)
- Two Serial Peripheral Interfaces (SPI)
- One Two Wire Interface (TWI, I^2C)
- One MultiMedia Card Interfaces
- JTAG debug port
- Digital Ports - up to 39 available
- Control Signals: IRQs, BMS, SHDN, WKUP
- 4 Programmable Clocks

Some of the various functions are realized by multiplexing connector pins; therefore not all functions may be used at the same time (see Appendix D, *Panel-Card Pin Assignment*)).

3.5. Miscellaneous

- Three 16-Bit Timer/Counter
- Real Time Timer (RTT), with battery backup support
- Periodic Interval Timer (PIT)
- Watchdog Timer (WDT)
- Unique Hardware Serial Number

3.6. Power Supply

- 3.3V power supply
- 3V backup power supply, e.g. from a lithium battery

3.7. Dimensions

- Panel-Card 35: 95.5 x 70 mmm (WxD)
- Panel-Card 57: 164 x 112 mmm (WxD)
- Panel-Card 70: 170.2 x 125 mmm (WxD)
- Desk70: 244 x 181,2 x 28,2/53,2 (Lx Bx H1/H2)

4. Hardware Description

4.1. Mechanics

The Panel-Card uses rugged and inexpensive 0.1″ headers as bus connectors which facilitate prototyping. The Panel-Card can such be placed even on a standard 0.1" pitch breadboard.

The size of the Panel-Card's PCB and the location of its mounting holes is adapted to the mechanics of standard 93x70mm LCDs, so the Panel-Card can easily be mounted in any enclosure which is prepared for such LCDs.

The position of the connectors, the board outline and the active area of the display is symmetrical in both x- and y-direction. This makes up for a simple, straight forward and unequivocal relationship between these parts in order to achieve a replaceability and upgradeability for different combinations of base boards, CPU cards, and displays.

4.2. Desk70

The Desk70 is a complete solution in a rugged aluminium housing. It consists of a Panel-Card70 and a Panel-Card Connector.

4.3. AT91SAM9261 Processor Core

The AT91SAM9261 runs at 200 MHz with a memory bus frequency of 100 MHz.

Here are some of the most important features of the Panel-Card ARM926EJ-S core:

- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
- 32 Bit Data Bus
- ARM v4 and v5 Memory Management Unit (MMU)
- ARM v5 32-bit Instruction Set, ARM Thumb 16-bit Instruction Set supported
- DSP Instruction Extensions
- ARM Jazelle® Technology for Java® Acceleration
- EmbeddedICE™ Debug Communication Channel Support

Some of these features - like Jazelle - are currently not supported by the operating system of the product.

4.4. Memory

The Panel-Card is equipped with 32-Bit CPU-bus which is not exported on the connectors but only used internally.

4.4.1. NOR Flash

The Panel-Card is equipped with a 16 MB or 64 MB NOR flash with 100000 erase and write cycles. It is organized in 128KB blocks. Customer specific adaptations are possible up to 128 MB on-board NOR flash. It is connected to chip select zero (NCS0) of the micro-controller.

The flash memory is made up of 1 or 2 ICs which have separated address spaces (see Appendix C, *Address Map (Physical Address Space)*).

Typically NOR flash is organized in blocks, similar to hard disks. Typical block sizes are 64, 128, 256 KB. NOR flash can be read and written randomly. This makes it possible to use NOR flash as execute in place (XIP) memory. To erase already written data, the whole block containing the data has to be erased.

NOR flash is subject to limited write and erase cycles. These are typically 100.000 cycles per block. So it is highly recommended to use wear levelling file systems.

4.4.2. SDRAM

The Panel-Card is equipped with 64MB SDRAM. Customer specific adaptations allow configurations up to 128MB. The SDRAM is connected to chip select one (NCS1) of the micro-controller.

SDRAM is volatile memory which allows random access to any location of its memory area. SDRAM has a synchronous interface. This means that it waits for a clock signal before responding to its control inputs, therefore it is synchronized with the CPU bus. The clock is used to drive a finite state machine in the chip, which allows to accept new instructions, before the previous one has finished executing.

4.4.3. EEPROM

The Panel-Card is equipped with a 256 bytes EEPROM, connected to the TWI (I^2C).

EEPROM stands for Electrically Erasable Programmable Read-Only Memory and is non-volatile memory, which is used to store small amounts of data like calibration or configuration data. EEPROMS are byte-wise erasable, thus allowing true random access.

4.4.4. SRAM

The Panel-Card's micro-controller is equipped with 160 KB internal SRAM. The internal SRAM can be accessed in one bus cycle and may be used for time critical sections of code or interrupt handlers.

4.4.5. DataFlash

The Panel-Card 57 and Panel-Card 70 are equipped with 128 KB DataFlash™.

DataFlash is a Atmel® proprietary interface and is compatible to the SPI standard. Similar to other flash chips it can be addressed page orientated and is available in sizes up to 8MB. Furthermore it is a possible boot media for the microcontroller.

4.5. Bus Matrix

The bus matrix of AT91SAM-controllers allows many master and slave devices to be connected independently of each other. Each master has a decoder and can be defined specially for each master. This allows concurrent access of masters to their slaves (provided the slave is available).

The bus matrix is thus the bridge between external devices connected to the EBI, the microcontroller's embedded peripherals and the CPU core.

Master 0	ARM926™ Instruction
Master 1	ARM926™ Data
Master 2	PDC
Master 3	LCD Controller
Master 4	USB Host DMA

Table 4.1. Bus Matrix Masters

Slave 0	Internal SRAM 160KB
Slave 1	Internal ROM
Slave 2	LCD Controller / USB Host User Interface
Slave 3	External Bus Interface (EBI)
Slave 4	Internal Peripherals

Table 4.2. Bus Matrix Masters

4.6. Advanced Interrupt Controller (AIC)

The core features of the Advanced Interrupt Controller are:

- 32 Internal or External Interrupt Sources
- 8-level Priority Controller
- Level Sensitive or Edge Triggered
- Programmable Polarity for External Sources

Moreover, all PIO lines can be used to generate a PIO interrupt. However, the PIO lines can only generate level change interrupts, that is, positive as well as negative edges will generate an interrupt. The PIO interrupt itself (PIO to AIC line) is usually programmed to be level-sensitive. Otherwise interrupts will be lost if multiple PIO lines source an interrupt simultaneously.

On the Panel-Card IRQ0, IRQ1 and IRQ2 are available. The list of peripheral identifiers which are used to program the AIC can be found in Table B.1, “Peripheral Identifiers”.

4.7. Battery Backup

The following parts of the AT91SAM9261 Processor can be backed-up by a battery:

- Slow Clock Oscillator
- Real Time Timer
- Reset Controller
- Shutdown Controller
- General Purpose Backup Registers

It is recommended to always use a backup power supply (normally a battery) in order to speed up the boot-up time and to avoid reset problems.

4.8. Reset Controller (RSTC)

The embedded microcontroller has an integrated Reset Controller which samples the backup and the core voltage. The presence of a backup voltage (VDDBU) when the card is powered down speeds up the boot time of the microcontroller.

4.9. Serial Number

Every Panel-Card has a unique 48-bit hardware serial number chip which can be used by application software. The chip is a Dallas® one-wire-chip. A Linux driver is provided.

4.10. Clock Generation

4.10.1. Processor Clocks

The CPU generates its clock signals based on two crystal oscillators: One slow clock (SLCK) oscillator running at 32.768 KHz and one main clock oscillator running at 18.432 MHz. The slow clock oscillator also serves as the time base for the real time timer. It draws a minimum of current (a few micro-Amps) and can therefore be backeded up by a small lithium battery when the board is powererd down.

From the main clock oscillator, the CPU generates two further clocks by using two PLLs. PLLA provides the processor clock (PCK) and the master clock (MCK). PLLB typically provides the 48 MHz USB clock and is normally used only for this purpose. The clocks of most peripherals are derived from MCK. These include EBI, USART, SPI, TWI, SSC, PIT and TC.

Some peripherals like the programmable clocks and the timer counters (TC) can also run on SLCK. The real time timer (RTT) always runs on SLCK.

Clock	Frequency	Source
PCK (Processor Clock)	200 MHz	PLLA
MCK (Master Clock)	100 MHz	PLLA/2
USB Clock	48 MHz	PLLB
Slow Clock	32.768 KHz	Slow Clock Oscillator

Table 4.3. AT91SAM9261 Clocks

4.10.2. Programmable Clocks

The programmable clocks can be individually programmed to derive their input from SLCK, PLLA, PLLB and Main Clock. Each PCK has a divider of 2, 4, 8, 16, 32 or 64.

The Panel-Card features four programmable clocks: PCK0, PCK1, PCK2 and PCK3.

4.11. Power Management Controller (PMC)

4.11.1. Function

The PMC has a Peripheral Clock register which allows to individually enable or disable the clocks of all integrated peripherals by using their "Peripheral Identifier" (see Table B.1, “Peripheral Identifiers”). The System Clock register allows to enable or disable each of the following clocks individually:

- Processor Clock
- LCD Clock (HCK1)
- USB Host Clock (common for both channels)
- USB Device Clock
- Programmable Clocks

The PMC status register provides "Clock Ready" or, respectively, "PLL Lock" status bits for each of these clocks. An interrupt is generated when any of these bits changes from 0 to 1. The PMC provides status flags for the

- Main Oscillator
- Master Clock
- PLLA
- PLLB
- Programmable Clocks

The Main Oscillator frequency can be measured by using the PMC Main Clock Frequency register. The SLCK is used as reference for the measurement.

4.11.2. Power Management

Using power management can dramatically reduce the power consumption of an Embedded Device. Via the PMC various clocks can be disabled or their speed can be reduced:

- stopping the PLLs (PLLA and / or PLLB)

- stopping the clocks of the various peripherals
- reducing the clock rates of peripherals, especially by changing MCK.

The PMC supports the following power-saving features: Idle mode and power-down mode. Please note that not every operating system supports these modes.

- **Idle Mode.** In idle mode, the processor clock will be re-enabled by any interrupt. The peripherals, however, are only able to generate an interrupt if they still have a clock, so care has to be taken as to when a peripheral can be powered down.
- **Power-down Mode.** In many cases a system waits for a user action or some other rare event. In such a case, it is possible to change MCK to SLCK. Any external event which changes the state on peripheral pins (not the USB) can then be detected by the PIO controller or the AIC.

  It should also be taken into account that when a PLL is stopped it will take some time to restart it. Changing the PLL frequencies or stopping them can therefore be done only at a moderate rate. If short reaction times are required, this is not a choice.

Additionally, the following measures can reduce power consumption considerably:

- switching off the TFT supply voltage
- putting peripheral chips like Ethernet controller and / or PHY or serial driver devices in power down mode
- putting the SDRAM into self-refresh mode

4.12. Real-time Timer (RTT)

The Real-time Timer is a 32-bit counter combined with a 16-bit prescaler running at Slow Clock (SLCK = 32768 Hz). As the RTT keeps running if only the backup supply voltage is available, it is used as a Real-time clock.

The RTT can generate an interrupt every time the prescaler rolls over. Usually the RTT is configured to generate an interrupt every second, so the prescaler will be programmed with the value 7FFFh.

The RTT can also generate an alarm if a preprogrammed 32-bit value is reached by the counter.

4.13. Timer Counter (TC)

The Panel-Card features one block of timer counters with three counters. None of them is available on the connectors. You can only use them internally.

The TC consists of three independent 16-bit Timer/Counter units. They may be cascaded to form a 32-bit or 48-bit timer/counter. The timers can run on the internal clock sources MCK/2, MCK/8, MCK/32, MCK/128, SLCK or the output of another timer channel. External clocks may be used as well as the counters can generate signals on timer events. They also can be used to generate PWM signals.

4.14. Periodic Interval Timer (PIT)

The PIT consists of a 20-bit counter running on MCK / 16. This counter can be preloaded with any value between 1 and 2^{20}. The counter increments until the preloaded value is reached. At this stage it rolls over and generates an interrupt. An additional 12-bit counter counts the interrupts of the 20 bit counter.

The PIT is intended for use as the operating system's scheduler interrupt.

4.15. Watchdog Timer

The watchdog timer is a 12-bit timer running at 256 Hz (Slow Clock / 128). The maximum watchdog timeout period is therefore equal to 16 seconds. If enabled, the watchdog timer asserts a hardware reset at the end of the timeout period. The application program must always reset the watchdog timer before the timeout is reached. If an application program has crashed for some reason, the watchdog timer will reset the system, thereby reproducing a well defined state once again.

The Watchdog Mode Register can be written only once. After a processor reset, the watchdog is already activated and running with the maximum timeout period. Once the watchdog has been reconfigured or deactivated by writing to the Watchdog Mode Register, only a processor reset can change its mode once again.

4.16. Peripheral DMA Controller (PDC)

The Peripheral DMA Controller (PDC) transfers data between on-chip serial peripherals and the on- and/or off-chip memories. The PDC contains unidirectional and bidirectional channels. The full-duplex peripherals feature unidirectional channels used in pairs (transmit only or receive only). The half-duplex peripherals feature one bidirectional channel. Typically full-duplex peripherals are USARTs, SPI or SSC. The MCI is a half duplex device.

The user interface of each PDC channel is integrated into the user interface of the peripheral it serves. The user interface of unidirectional channels (receive only or transmit only), contains two 32-bit memory pointers and two 16-bit counters, one set (pointer, counter) for current transfer and one set (pointer, counter) for next transfer. The bidirectional channel user interface contains four 32-bit memory pointers and four 16-bit counters. Each set (pointer, counter) is used by current transmit, next transmit, current receive and next receive.

Using the PDC removes processor overhead by reducing its intervention during the transfer. This significantly reduces the number of clock cycles required for a data transfer, which improves microcontroller performance. To launch a transfer, the peripheral triggers its associated PDC channels by using transmit and receive signals. When the programmed data is transferred, an end of transfer interrupt is generated by the peripheral itself. There are four kinds of interrupts generated by the PDC:

- End of Receive Buffer
- End of Transmit Buffer

- Receive Buffer Full
- Transmit Buffer Empty

The "End of Receive Buffer" / "End of Transmit Buffer" interrupts signify that the DMA counter has reached zero. The DMA pointer and counter register will be reloaded from the reload registers ("DMA new pointer register" and "DMA new counter register") provided that the "DMA new counter register" has a non-zero value. Otherwise a "Receive Buffer Full" or, respectively, a "Transmit Buffer Empty" interrupt is generated, and the DMA transfer terminates. Both reload registers are set to zero automatically after having been copied to the DMA pointer and counter registers.

4.17. Debug Unit (DBGU)

The Debug Unit is a simple UART which provides only RX/TX lines. It is used as a simple serial console for Firmware and Operating Systems.

4.18. JTAG Unit

The JTAG unit can be used for hardware diagnostics, hardware initialization, flash memory programming, and debug purposes. The JTAG unit supports two different modes, namely the "ICE Mode", and the "Boundary Scan" mode. It is normally jumpered for "ICE Mode".

JTAG interface devices are available for the unit. However, the use of them is not within the scope of this document.

4.19. Two-wire Interface (TWI)

The TWI is also known under the expression "I^2C-Bus", which is a trademark of Philips and may therefore not be used by other manufacturers. However, interoperability is guaranteed. The TWI supports both master or slave mode.

The TWI uses only two lines, namely serial data (SDA) and serial clock (SCL). According to the standard, the TWI clock rate is limited to 400 kHz in fast mode and 100 kHz in normal mode, but configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

4.20. Multimedia Card Interface (MCI)

The Panel-Card features two Multimedia Card Controller, of which MCI-A is externally available on the connectors. On the Evaluation Board of the Panel-Card 35, it is connected to the SD/MMC-Card slot. Please note that operating systems like Linux do not necessarily support all features of the hardware unit.

The MultiMedia Card Interface (MCI) supports the MultiMedia Card (MMC) Specification V3.11, the SDIO Specification V1.1 and the SD Memory Card Specification V1.0.

The MCI includes a command register, response registers, data registers, timeout counters and error detection logic that automatically handle the transmission of commands and, when required, the reception of the associated responses and data with a limited processor overhead. The MCI supports stream, block and multi-block data read and

write, and is compatible with the Peripheral DMA Controller (PDC) channels, minimizing processor intervention for large buffer transfers.

The MCI operates at a rate of up to Master Clock divided by 2 and supports the interfacing of 2 slot(s). Each slot may be used to interface with a MultiMediaCard bus (up to 30 Cards) or with a SD Memory Card. Only one slot can be selected at a time (slots are multiplexed). A bit field in the SD Card Register performs this selection.

The SD Memory Card communication is based on a 9-pin interface (clock, command, four data and three power lines) and the MultiMedia Card on a 7-pin interface (clock, command, one data, three power lines and one reserved for future use). The SD Memory Card interface also supports MultiMedia Card operations. The main differences between SD and MultiMedia Cards are the initialization process and the bus topology.

4.21. USB Host Port (UHP)

The Panel-Card integrates two USB host ports supporting speeds up to 12 MBit/s.

The USB Host Port (UHP) interfaces the USB with the host application. It handles Open HCI protocol (Open Host Controller Interface) as well as USB v2.0 Full-speed and Low-speed protocols.

The USB Host Port integrates a root hub and transceivers on downstream ports. It provides several high-speed half-duplex serial communication ports. Up to 127 USB devices (printer, camera, mouse, keyboard, disk, etc.) and an USB hub can be connected to the USB host in the USB "tiered star" topology.

4.22. USB Device Port (UDP)

The Panel-Card integrates one USB device port supporting speeds up to 12 MBit/s.

The USB Device Port (UDP) is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification. The USB device port enables the product to act as a device to other host controllers.

The USB device port can also be implemented to power on the board. One I/O line may be used by the application to check that VBUS is still available from the host. Self-powered devices may use this entry to be notified that the host has been powered off. In this case, the pullup on DP must be disabled in order to prevent feeding current to the host. The application should disconnect the transceiver, then remove the pullup.

4.23. Universal Sychronous Asynchronous Receiver and Transmitter (USART)

The Panel-Card has up to three independent USARTs, not including the debug unit.

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the

transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

The USART supports the connection to the Peripheral DMA Controller, which enables data transfers to the transmitter and from the receiver. The PDC provides chained buffer management without any intervention of the processor.

Six different modes are implemented within the USARTs:

- Normal (standard RS232 mode)
- RS485
- Hardware Handshaking
- ISO7816 Protocol: T=0 or T=1
- IrDA

RS485. In RS485 operating mode the RTS pin is automatically driven high during transmit operations. If RTS is connected to the "enable" line of the RS485 driver, the driver will thus be enabled only during transmit operations.

Hardware Handshaking. The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS. The receive DMA channel must be active for this mode. The RTS signal is driven high if the receiver is disabled or if the DMA indicates a buffer full condition. As the RTS signal is connected to the CTS line of the connected device, its transmitter is thus prevented from sending any more characters.

ISO7816. The USARTs have an ISO7816-compatible mode which permits interfacing with smart cards and Security Access Modules (SAM). Both T=0 and T=1 protocols of the ISO7816 specification are supported.

IrDA. The USART features an infrared (IrDA) mode supplying half-duplex point-to-point wireless communication. It includes the modulator and demodulator which allows a glueless connection to the infrared transceivers. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 kb/s to 115.2 kb/s.

Signals of the Serial Interfaces. All UARTs/USARTs have one receiver and one transmitter data line (full duplex). Not all USARTs are implemented with full modem control lines. Furthermore the available lines depend largely on the used multiplexing. Most modem control lines can be implemented with standard digital ports.

Hardware Interrupts. There are several interrupt sources for each USART:

- Receive: RX Ready, (DMA) Buffer Full, End of Receive Buffer
- Transmit: TX Ready, (DMA) Buffer Empty, End of Transmit Buffer, Shift Register Empty
- Errors: overrun, parity, framing, and timeout errors
- Handshake: the status of CTS has changed

- Break: the receiver has detected a break condition on RXD
- NACK: non acknowledge (ISO7816 mode only)
- Iteration: the maximum number of repetitions has been reached (ISO7816 mode only)

Please refer to the chapter about the DMA unit (PDC) for a description of the "Buffer Full" and "End of Receive / Transmit Buffer" events.

4.24. Synchronous Peripheral Interface (SPI)

The Panel-Card features two externally available SPI ports, each with three chip selects. Be aware that on the Panel-Card 35 when connected to the Evaluation Board and on the Panel-Card 57/70 all chip selects of the second port are already used. To compensate for this, you can also use GPIO pins as chip selects with the Linux SPI driver. Additionally the first SPI port is multiplexed with the MMC controller.

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPIs. During a data transfer, one SPI system acts as the "master" which controls the data flow, while the other devices act as "slaves" which have data shifted into and out by the master.

A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS). The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master may transmit data at a variety of baud rates; the SPCK line cycles once for each bit that is transmitted. The SPI baudrate is Master Clock (MCK) divided by a value between 1 and 255
- Slave Select (NSS): This control line allows slaves to be turned on and off by hardware.

Each SPI Controller has a dedicated receive and transmit DMA channel.

4.25. Peripheral Input/Output Controller (PIO)

The Panel-Card has a maximum of 40 freely programmable digital I/O ports on its connectors. These pins are also used by other peripheral devices.

The Parallel Input/Output Controller(PIO) manages up to 32 programmable I/O ports. Each I/O port is associated with a bit number in the 32 bit register of the user interface. Each I/O

port may be configured for general purpose I/O or assigned to a function of an integrated peripheral device. In doing so multiplexing with multiple integrated devices is possible. That means a pin may be used as GPIO or only as one of the peripheral functions. The PIO Controller also features a synchronous output providing up to 32 bits of data output in a single write operation.

The following characteristics are individually configurable for each PIO pin:

- PIO enable
- Peripheral enable
- Output enable
- Output level
- Write Enable
- Level change interrupt
- Glitch filter: pulses that are lower than a half clock cycle are ignored
- Open-drain outputs
- Pull-up resistor

All configurations as well as the pin status can be read back by using the appropriate status register. Multiple pins of each PIO can also be written simultaneously by using the synchronous output register.

For interrupt handling, the PIO Controllers are considered as user peripherals. This means that the PIO Controller interrupt lines are connected among the interrupt sources 2 to 31. Refer to the PIO Controller peripheral identifier Table B.1, “Peripheral Identifiers” to identify the interrupt sources dedicated to the PIO Controllers. The PIO Controller interrupt can be generated only if the PIO Controller clock is enabled.

A number of the PIO signals might be used internally on the module. Care has to be taken when accessing the PIO registers in order not to change the settings of these internal signals, otherwise a system crash is likely to happen.

4.26. LCD controller

The LCD controller of the AT91SAM9261 (theoretically) supports displays with a resolution of up to 2048x2048 with a color depth of up 24 bits per pixel.

The LCD controller relies on a relatively simple frame buffer concept, which means that all graphics and character functions have to be implemented in software: character sets and graphic primitives are not integrated in the controller.

4.26.1. LCDC Initialisation and LCD Power Sequencing

LCD cells (pixels) should not be subjected to DC power for prolonged periods of time, as chemical decomposition might take place. The LCD controller therefore provides for

a strict AC control of the LCD pixels. To do so, the LCD controller has to be initialized appropriately. Switching on the LCD supply voltage therefore has to take place after the LCDC initialization or shortly before.

Accordingly, the LCDC should not be powered down without deactivating the LCD supply voltage. The same is true if the LCDC is stopped indirectly by stopping the respective clock source, namely the PLLA.

The LCD backlight supply is not involved in these considerations. It may switched on or off at any time independently of the state of the LCDC.

4.26.2. LCDC Video Memory Selection

The video memory of the LCDC is part of the working memory of the processor. It might either reside in the internal SRAM, as well as in the external SDRAM. Using the internal SRAM has the advantage that the LCDC can access its video memory via an autonomous bus and does not affect the processor performance. However, as the internal SRAM has a capacity of only 160 kBytes, the color depth for a QVGA display is only 16 bit / pixel (320 x 240 x 2 = 153600 bytes are necessary). For a high quality display 16 bit per pixel might not be sufficient.

On the other hand, using the SDRAM as video memory has the advantage that there is plenty of space for all resolutions. Also the internal SRAM is now available for time critical software sections. Of course the LCDC will now be permanently scanning its video memory and might therefore reduce the overall performance to some degree.

4.26.3. LCDC Frame Buffer

The LCDC video memory is organized as a frame buffer in a straight forward way. It supports color depths of 1, 2, 4, 8, 16, or 24 bit per pixel. The video data is stored in a packed form with no unused bits in the video memory.

The color resolutions of 1, 2, 4, and 8 bpp (bits per pixel) use a palette table which is made up of 16-bit entries. The value of each pixel in the frame buffer serves as an index into the palette table. The value of the respective palette table entry is output to the display by the LCDC, see Table 4.4, “LCDC palette entry”.

Bit[14..10]	Bit[9..5]	Bit[4..0]
Blue[7..3]	Green[7..3]	Red[7..3]

Table 4.4. LCDC palette entry

The bits 2..0 of each color channel are not used in the palettized configuration — they are set to 0. The intensity bit sets the least significant valid bits of every color, that is, the bits 2, 10, and 18 of a 24-bit LCDC output word.

The same scheme as above is used in the 16-bit color resolution configuration, although in this case the frame buffer entry is output directly to the display instead of indexing a palette table.

In the 24-bit color resolution configuration, each frame buffer entry consists of one byte for each color, see Table 4.5, “LCDC 24 bit memory organization”.

Bit[23..16]	Bit[15..8]	Bit[7..0]
Blue[7..0]	Green[7..0]	Red[7..0]

Table 4.5. LCDC 24 bit memory organization

The "BGR" (blue-green-red) sequence in the AT91SAM9261 LCDC is not frequently used by graphics libraries or bitmaps ("RGB" is more of a standard), neither is the use of bit 15 as an intensity bit. Of course, the first problem can be circumvented by connecting the LCDC lines to the LCD in a way deviating from the Atmel designation, that is, by exchanging the "blue" against the "red" lines.

The Linux frame buffer driver offers a function which returns the information about the frame buffer structure including the assignment of each frame buffer bit to a color channel bit. It is recommended that graphics software uses this function in order to achieve a correct color representation.

4.27. Display (TFT)

Panel-Cards with the following displays are available:

- ET035005DM6 (3,5″, 320x240, BGR)
- ET057011DHU (5,7″, 320x240, RGB)
- ET057009DHU (5,7″, 640x480, RGB)

All TFTs have a LED backlight which can be dimmed and switched off. Panel-Cards with ET035005DM6 use PIO ports PC4 and PC5 to dim the backlight and it is switched off with PC1. PC10 is used to switch off the TFT power supply. On the other Panel-Cards, the backlight is dimmed by the contrast value of the LCDC. Both the backlight and the TFT power supply is switch off with PC10.

4.28. Touchscreen

The Panel-Card 35 is available with a touch. However, it does not have a touch controller on board, so it has to be implemented on the base board. A reference implementation with an ADS7843 touch controller can be found on the Panel-Card Evaluation board.

Panel-Card 57/70 always have a touchscreen and use the ADS7846 touch controller.

4.29. Ethernet Controller

The product is equipped with a Davicom DM9000A 10/100 MBit Ethernet Controller and a 10/100 MBit Twisted-Pair Magnetic Module (transformer plus filter).

An individual 48-bit MAC address (ETHERNET hardware address) is allocated to each product. This number is stored in flash memory. It is recommended not to change the MAC address in order to comply with IEEE Ethernet standards.

4.30. Buttons

The Panel-Card 57/70 have five buttons connected to PIO pins PA17-PA21.

5. Design Considerations

5.1. USB Host Controller (UHP)

External Parts. A few external parts are required for the proper operation of the UHP:

- With Panel-Card 35, pull-down resistors on each line of approximately 15 kΩ. These should be installed even if the UHP is not to be used at all in order to keep the signals from floating. Panel-Card 57 and Panel-Card 70 don't need them.
- With Panel-Card 35, series resistors of 27 Ω (5%) on each line. Panel-Card 57 and Panel-Card 70 don't need them.
- Small capacitors (e.g. 15pF) to ground on each line (optional).
- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.
- A circuit to generate the 5V VBUS supply voltage.

V_{BUS} considerations for USB Host. A USB host port has to provide a supply voltage V_{BUS} of 5V +- 5% which has to be able to source a maximum of 500mA, or 100mA in case of battery operation. Please refer to the appropriate rules in the USB specification. A low ESR capacitor of at least 120µF has to be provided on V_{BUS} in order to avoid excessive voltage drops during current spikes.

V_{BUS} has to have an over-current protection. The over-current drawn temporarily on V_{BUS} must not exceed 5A. Polymeric PTCs or solid state switches are recommended by the specification. Suitable PPTCs are "MultiFuse" (Bourns), "PolyFuse" (Wickmann/Littelfuse), "PolySwitch" (Raychem/Tyco).

It is required that the over-current condition can be detected by software, so that V_{BUS} can be switched off or be reduced in power in such a case.

Layout considerations. If external resistors are needed, they should be placed in the vicinity of the module's connector. The two traces of any of the differential pairs (USB-Host A+ and USB-Host A- , as well as USB-Host B+ and USB-Host B-) should not encircle large areas on the base board, in order to reduce signal distortion and noise. The are preferably routed closely in parallel to the USB connector.

USB High-Speed. If designing USB High-Speed a wave impedance of 90 Ω on the traces should be respected. The traces shoud be routed as short as possible and in parallel with as low parallel capacitance as possible.

5.2. USB Device Controller (UDP)

External Parts. A few external parts are required for the proper operation of the UDP:

- With Panel-Card 35, pull-down resistors on each line of approximately 330 kΩ. These should be installed even if the UDP is not to be used at all in order to keep the signals from floating. Panel-Card 57 and Panel-Card 70 don't need them.

- With Panel-Card 35, series resistors of 27 Ω (5%) on each line. Panel-Card 57 and Panel-Card 70 don't need them.

- A voltage divider on the 5V USB supply voltage VBUS converting this voltage to 3.3V (1.8V), e.g. 27 kΩ / 47 kΩ, for the VBUS monitoring input (USB_CNX).

- ESD protection devices are recommended for applications which are subject to external contact. The restrictions with regard to capacitive loading have to be applied when selecting a protection device.

The USB specification demands a switchable pull-up resistor of 1.5 kΩ on USB-Device+ which identifies the UDP as a full speed device to the attached host controller. On this module, this resistor is integrated on the chip. It can be switched on or off using the "USB Pad Pull-up Control Register", which is part of the "Bus Matrix User Interface" (not the "USB Device Port User Interface", as one might expect). This pull-up resistor is required to be switchable in order not to source current to an attached but powered down host. This would otherwise constitute an irregular condition on the host. The software has to take care of this fact.

The capacitors are intended to improve the signal quality (edge rate control) depending on the specific design. They are not mandatory. The total capacitance to ground of each USB pin, the PCB trace to the series resistor, and the capacitor must not exceed 75pF.

Operation with V_{BUS} as a Supply. Special care has to be taken if the module is powered by the VBUS supply. Please refer to the appropriate rules in the USB specification with regard to inrush current limiting and power switching. As the module draws more than 100mA in normal mode, it is a "high-power" device according to the specification (<100mA = "low-power", 100..500mA = "high-power"). It therefore requires staged switching which means that at power-up it should draw not more than 100mA on VBUS. The capacitive load of a USB device on VBUS should be not higher than 10µF.

Layout considerations. The external resistors should be placed in the vicinity of the module's connector. The traces of the differential pair (USB-Device+ and USB-Device-) should not encircle large areas on the base board, in order to reduce signal distortion and noise. The are preferably routed closely in parallel to the USB connector.

5.3. Ethernet Controller

Please take care of the specific layout requirements of the Ethernet port when designing a base board. The two signals of the transmitter pair (ETX+ and ETX-) should be routed in parallel (constant distance, e.g. 0.5mm) with no vias on their way to the RJ45-jack. The same is true for the receiver pair (ERX+ and ERX-). No other signals should be crossing or get next to these lines. If a ground plane is used on the base board, it should be omitted in the vicinity of the Ethernet signals.

A 1nF / 2kV capacitor should be connected between board ground and chassis ground (which is usually connected to the shield of the RJ45-jack).

Two LED outputs from the DM9000A controller can be used on the base board. LED_S indicates the current speed of the Ethernet connection (100MBit = on, 10 MBit = off).

LED_L indicates the combined link and carrier sense signal (LED mode 1 of the DM9000A), or only the carrier sense signal (LED mode 0).

5.4. Display

When designing a housing for the Panel-Card 57/70, care must be taken. The touch panel has a very sensitive area which should not be pressed to prevent performance degradation or malfunction. Please consult the manual of the corresponding displays.

6. Panel-Card Starterkit

6.1. Starterkit Contents

The Panel-Card 35 Starterkit contains the following components:

- Panel-Card 35
- Panel-Card EVB: Evaluation and Prototyping Board

The Panel-Card 57/70 Starterkit contains the following components:

- Panel-Card 57 or 70
- Panel-Card Connector

Additionally, Starterkits for all products contain the following components:

- Wall Adapter Power Supply, Input AC 230V, Output DC 9 to 16V, min. 400 mA
- Serial "Null-Modem" Cable with two 9-pin D-type Connectors
- Adapter cable for accessing the Debug UART
- CD with Operating System, Toolchain, and Documentation

6.2. Panel-Card EVB

The Panel-Card EVB (Evaluation Board) is designed to be both simple and universal. Some elements of the circuit board will not always be needed, but facilitate implementation for certain purposes. It was designed to serve the Panel-Card and other products as an evaluation platform.

6.2.1. First Steps

The Starter Kit board "Panel-Card EVB" makes it easy to put the module to use. The first steps involve the following:

- connecting the wall adapter to the main supply and to the board
- connecting the DBGU-Adapter and the serial cable to a COM port of a PC
- starting a terminal program for the selected COM port at 115200 baud, 8N1
- starting the module by flipping the power switch
- boot messages of the module are now expected to appear on the terminal

6.2.2. Power Supply

From an unregulated input voltage between 8 and 35V two voltages are produced:

- 3.3V for the CPU module,
- 5V for USB and optional peripherals

6.2.3. RS232 Interface

The RS232 port provides RS232 drivers/receivers for the RxD, TxD, RTS, CTS, RI and DCD signals of the one USART of the module. It is connected to X4 DSUB-9 connector on the EVB.

The RxD and TxD lines of the module's "Debug UART" are connected to X25 Debug on EVB. To use the console port of the Stamp9261, which usually is identical to the Debug UART, the serial adaptor cable has to be used. It connects the PC's TxD, RxD, and Ground lines to the appropriate pins of X25 Debug of the EVB.

6.2.4. Connectors

The following connectors are part of the Panel-Card EVB:

- Two 40-pin header connectors (0.1 inch pitch)
- Ethernet 10/100 MBit
- USB Host (dual)
- USB Device
- RS232
- MMC-Card Slot
- Matrix keyboard
- JTAG
- User Connector D-type 25pin
- User Connector 26pin header (optional)
- 2-contact terminal block for power supply
- DC connector for power supply

6.2.5. Rotary Encoder

The Panel-Card EVB includes a rotary encoder with push-button which is a "Human Interface Device" well suited for many embedded applications. Generally spoken, it is a simplified replacement for a computer mouse, touch pad, or keyboard. The rotary encoder represents a pointing device with only one dimension, while the push-button serves as a "return" key or mouse button.

The rotary encoder is accessed by two PIO ports of the module (see circuit diagram). The push-button occupies another PIO port.

6.2.6. Touch Controller

The Panel-Card EVB implements a ADS7843 Touch controller. It is connected to SPI of the module. The touch controller and the rotary encoder can only be used mutually exclusive. Connect jumper J2 to ID for the rotary encoder and to TP for touch.

6.2.7. Schematics

The following circuit diagram is intended for reference only and does not dispense the user from checking and applying the appropriate standards. No warranty can be granted if parts of the circuit are used in customer applications.

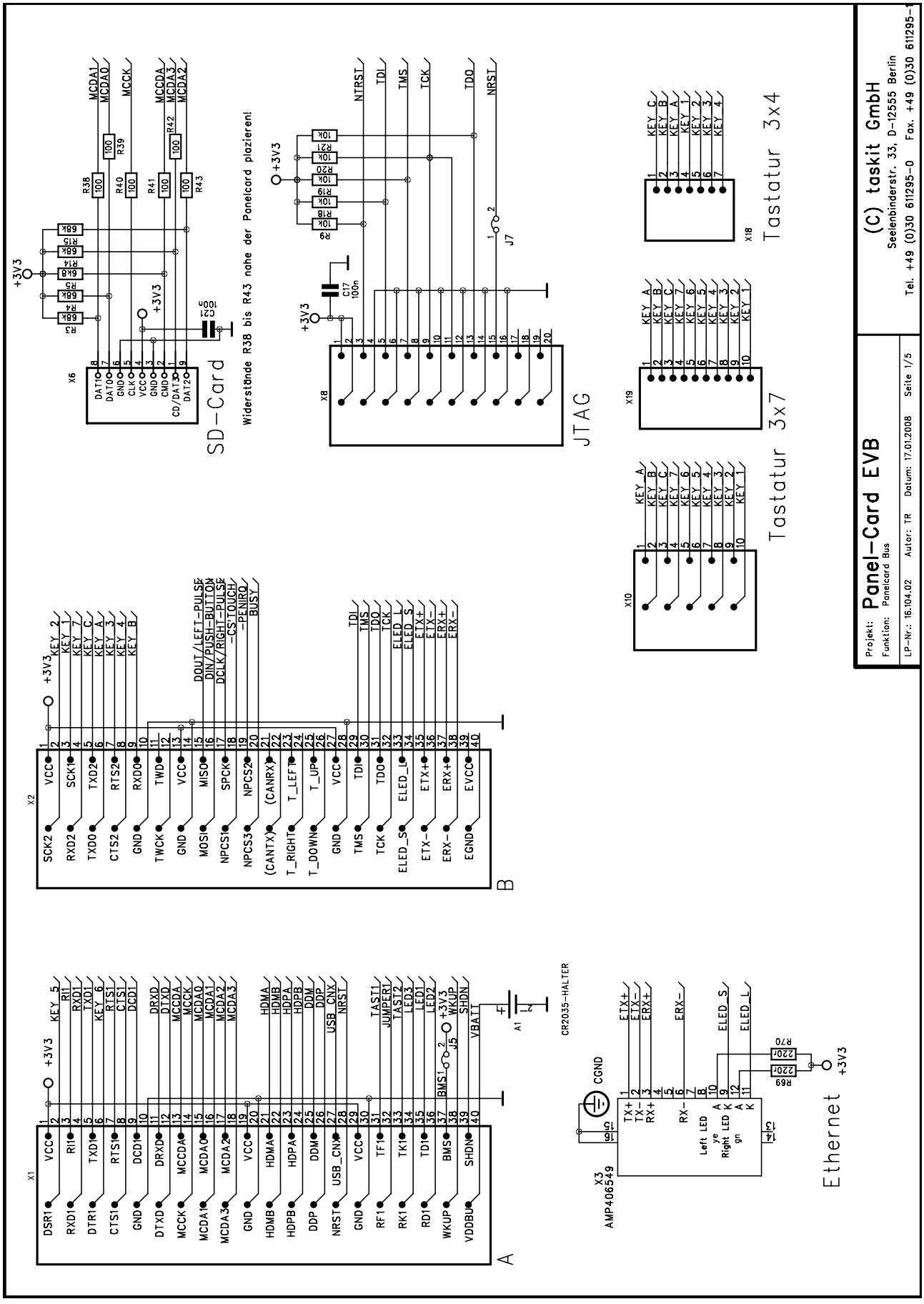

Figure 6.1. Panel-Card EVB Schematics Bus/JTAG

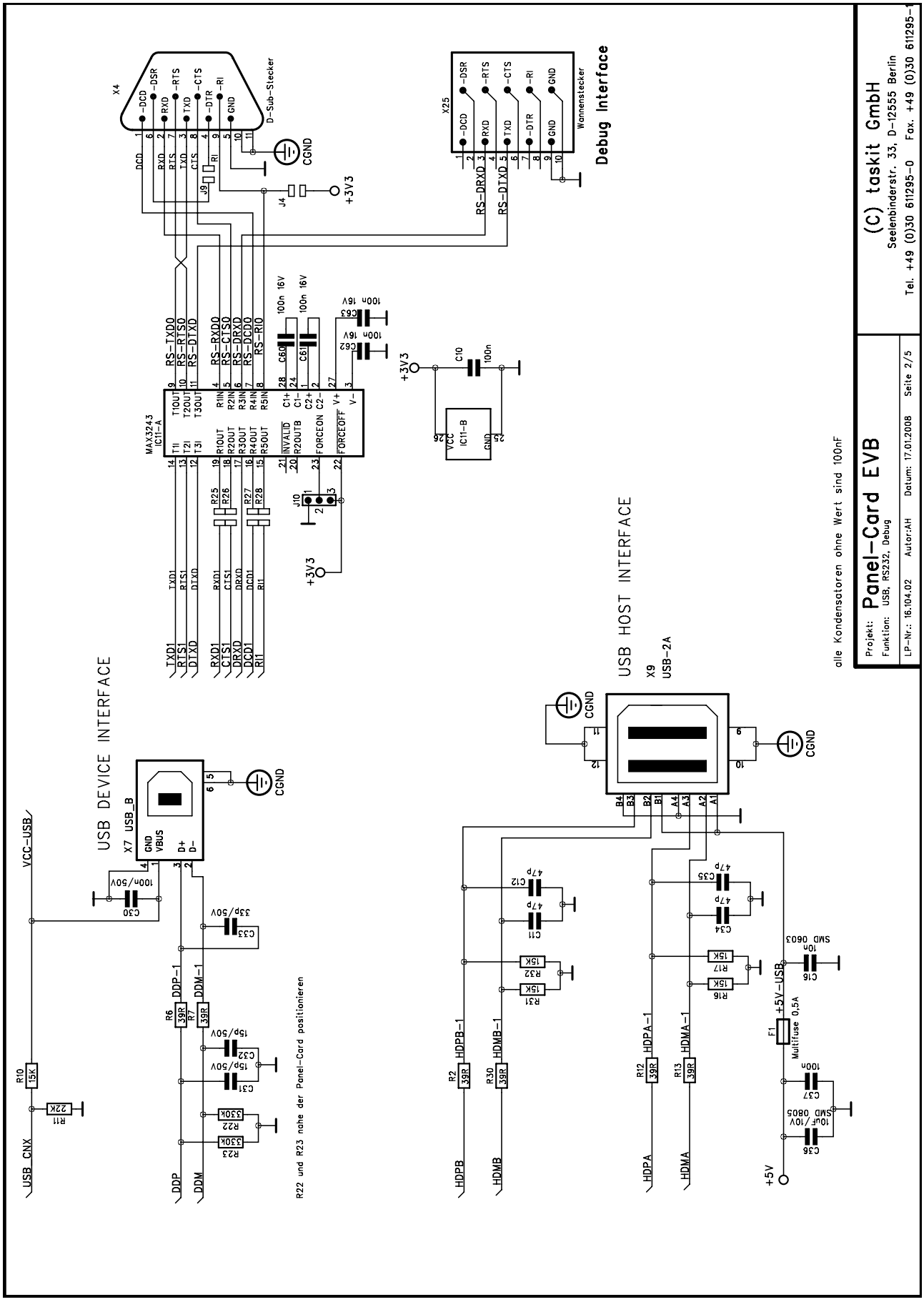

Figure 6.2. Panel-Card EVB Schematics USB/RS232

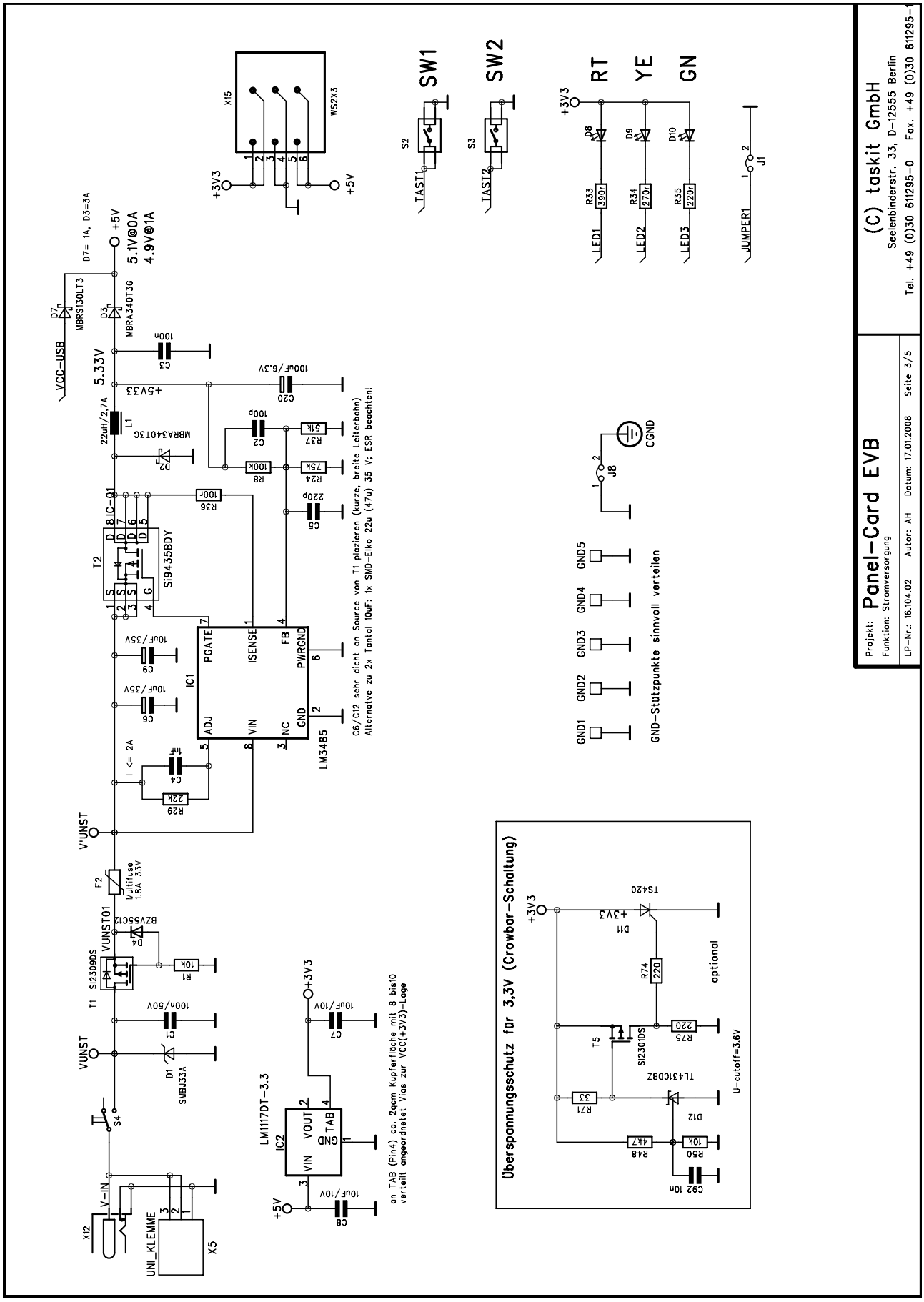

Figure 6.3. Panel-Card EVB Schematics Power Regulation

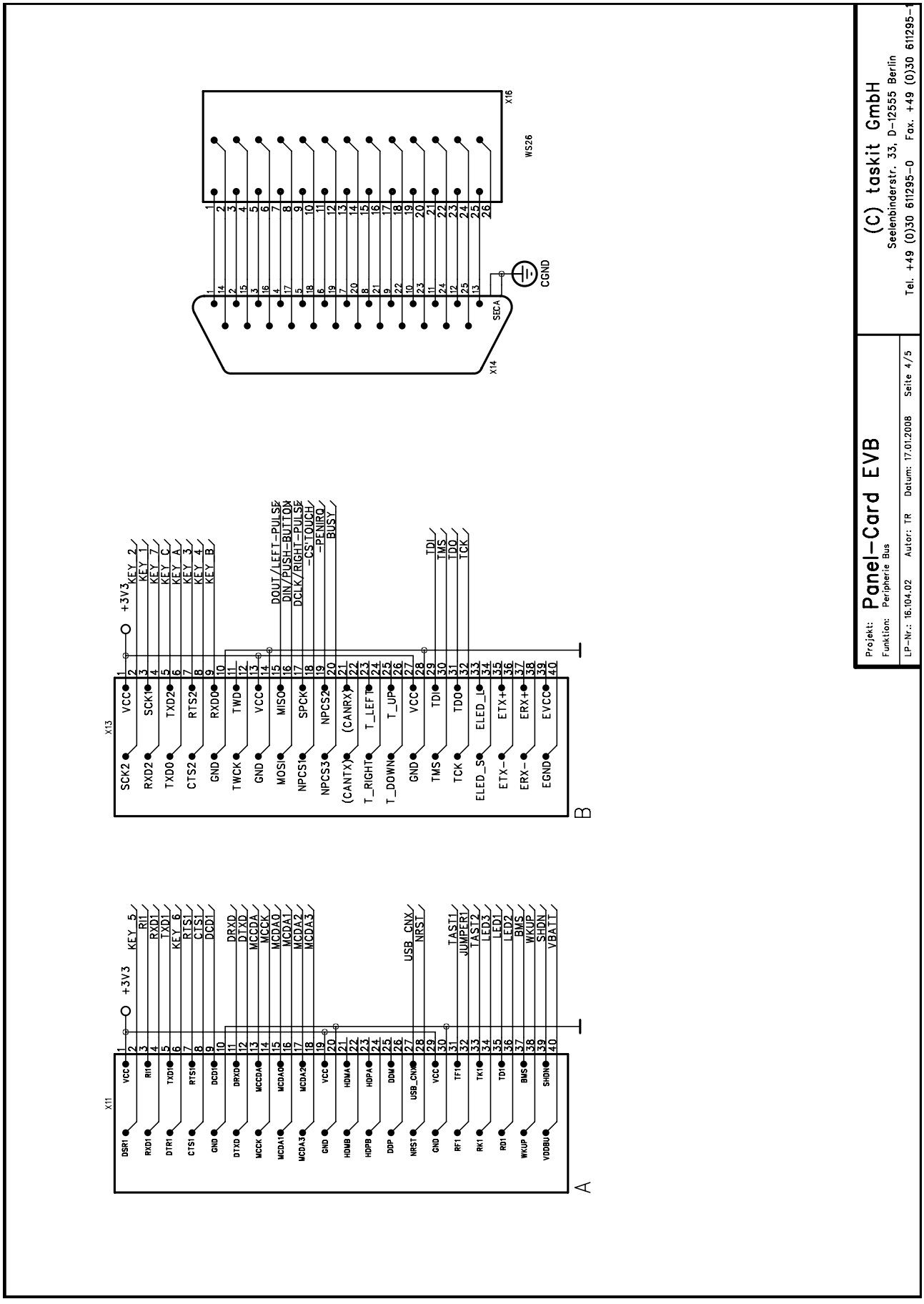

Figure 6.4. Panel-Card EVB Schematics Connectors

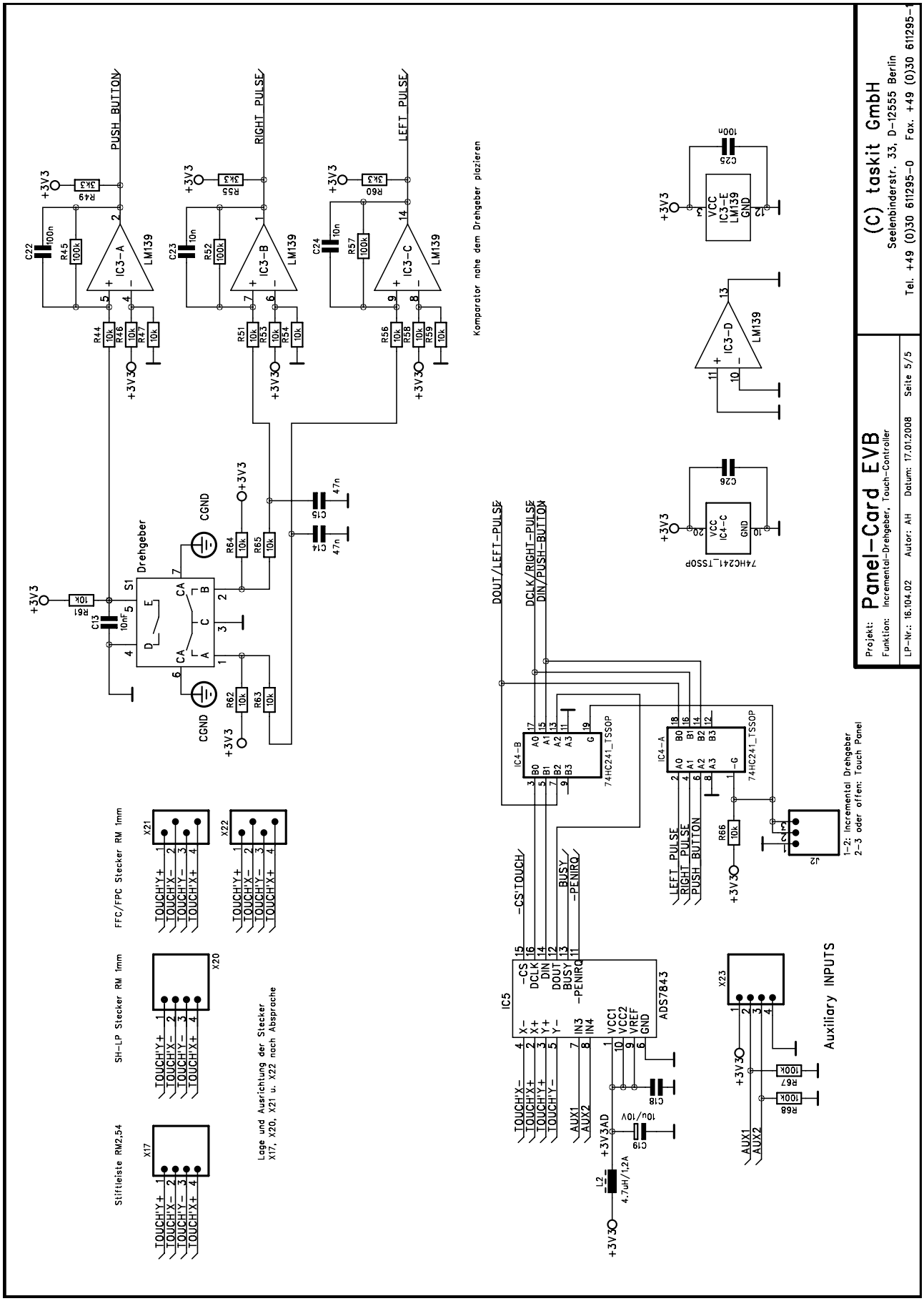

Figure 6.5. Panel-Card EVB Schematics HID

6.3. Panel-Card Connector

The Panel-Card Connector was designed to serve the Panel-Card 57/70 as an evaluation platform and as a deployable base board for all Panel-Cards. It can also be used to develop and deploy Stamp9261 and Stamp9G20 systems.

6.3.1. First Steps

The Panel-Card Connector makes it easy to put the Panel-Card/Stamp to use. The first steps involve the following:

- connecting the board to the Panel-Card/Stamp-Adaptor according to Figure 6.6, “Panel-Card Connector setup”
- connecting the wall adapter to the main supply and to the board
- connecting RS232 IF-Module via the serial cable to a COM port of a PC
- starting a terminal program for the selected COM port at 115200 baud, 8N1
- starting the module by flipping the power switch
- boot messages of the module are now expected to appear on the terminal

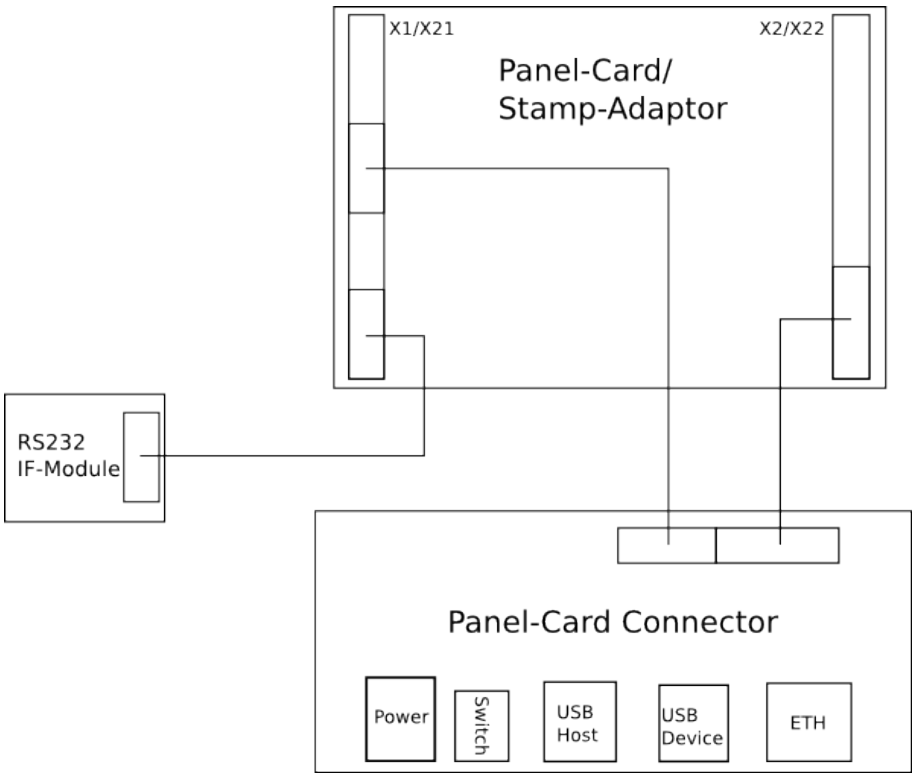

Figure 6.6. Panel-Card Connector setup

6.3.2. Power Supply

From an unregulated input voltage between 8 and 35V two voltages are produced:

- 3.3V for the CPU module

- 5V for USB

6.3.3. Connectors

The following connectors are part of the Panel-Card Connector

- Two 40-pin header connectors (0.1 inch pitch)
- Ethernet 10/100 MBit
- USB Host (dual)
- USB Device
- RS232 for use with an RS232 IF-Module
- DC connector for power supply

6.3.4. Dimensions

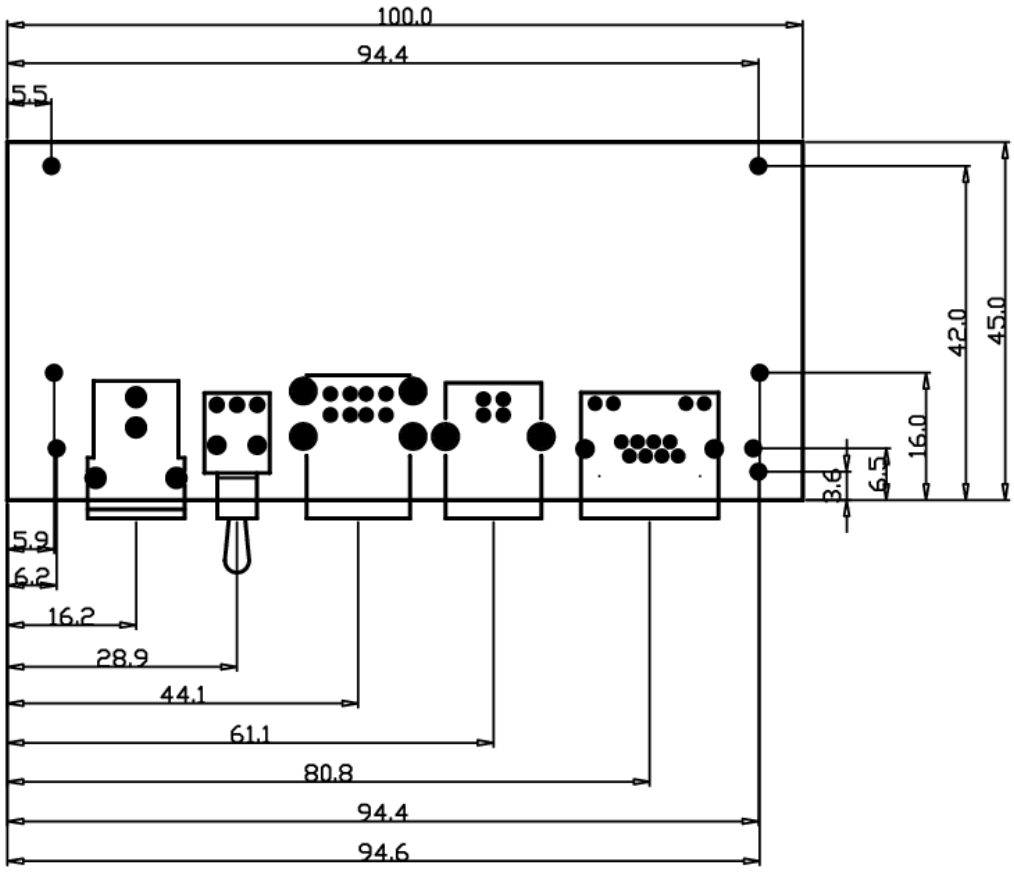

Figure 6.7. Panel-Card Connector Dimensions

6.3.5. Schematics

The following circuit diagram is intended for reference only and does not dispense the user from checking and applying the appropriate standards. No warranty can be granted if parts of the circuit are used in customer applications.

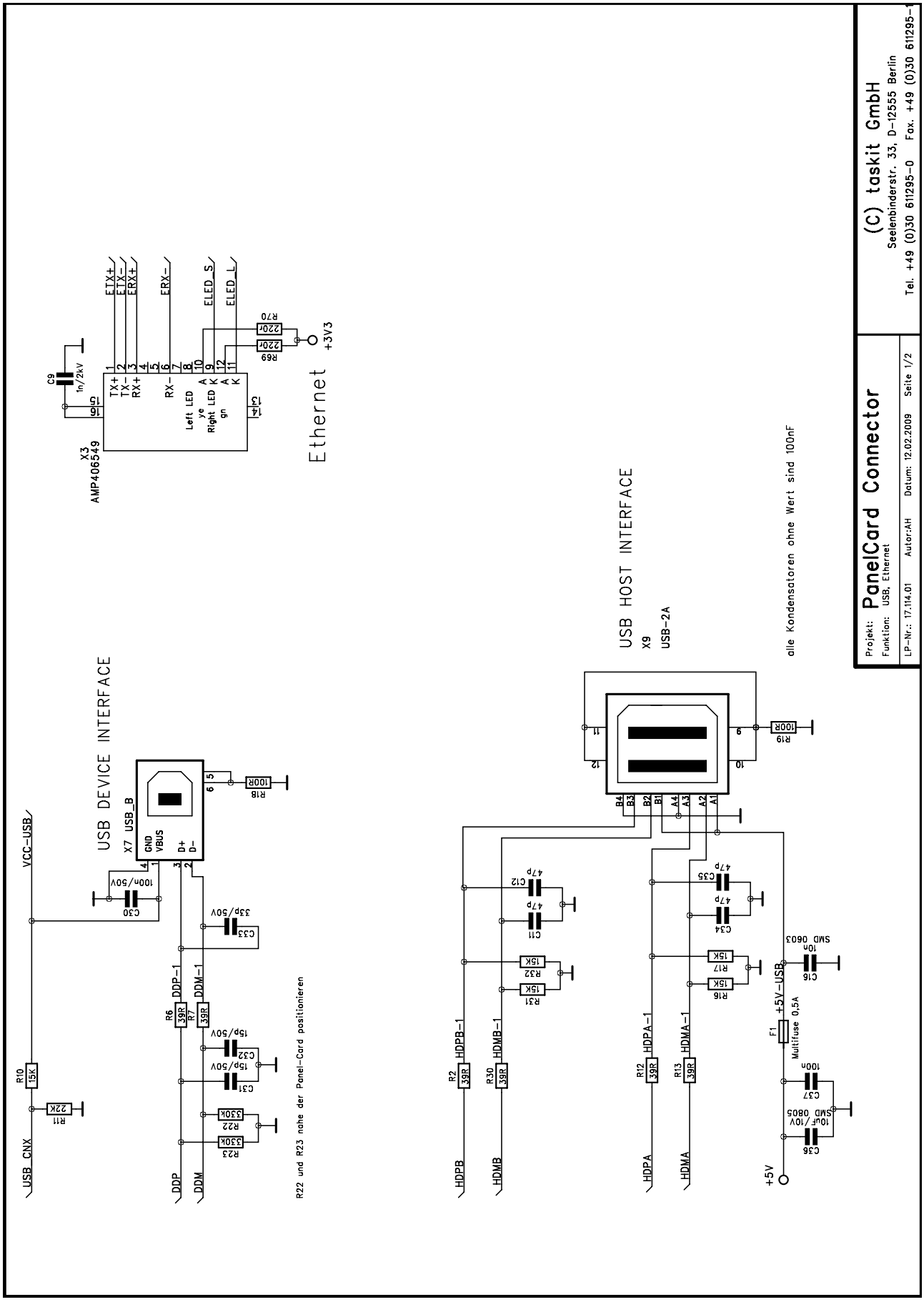

Figure 6.8. Panel-Card Connector Schematics USB/Ethernet

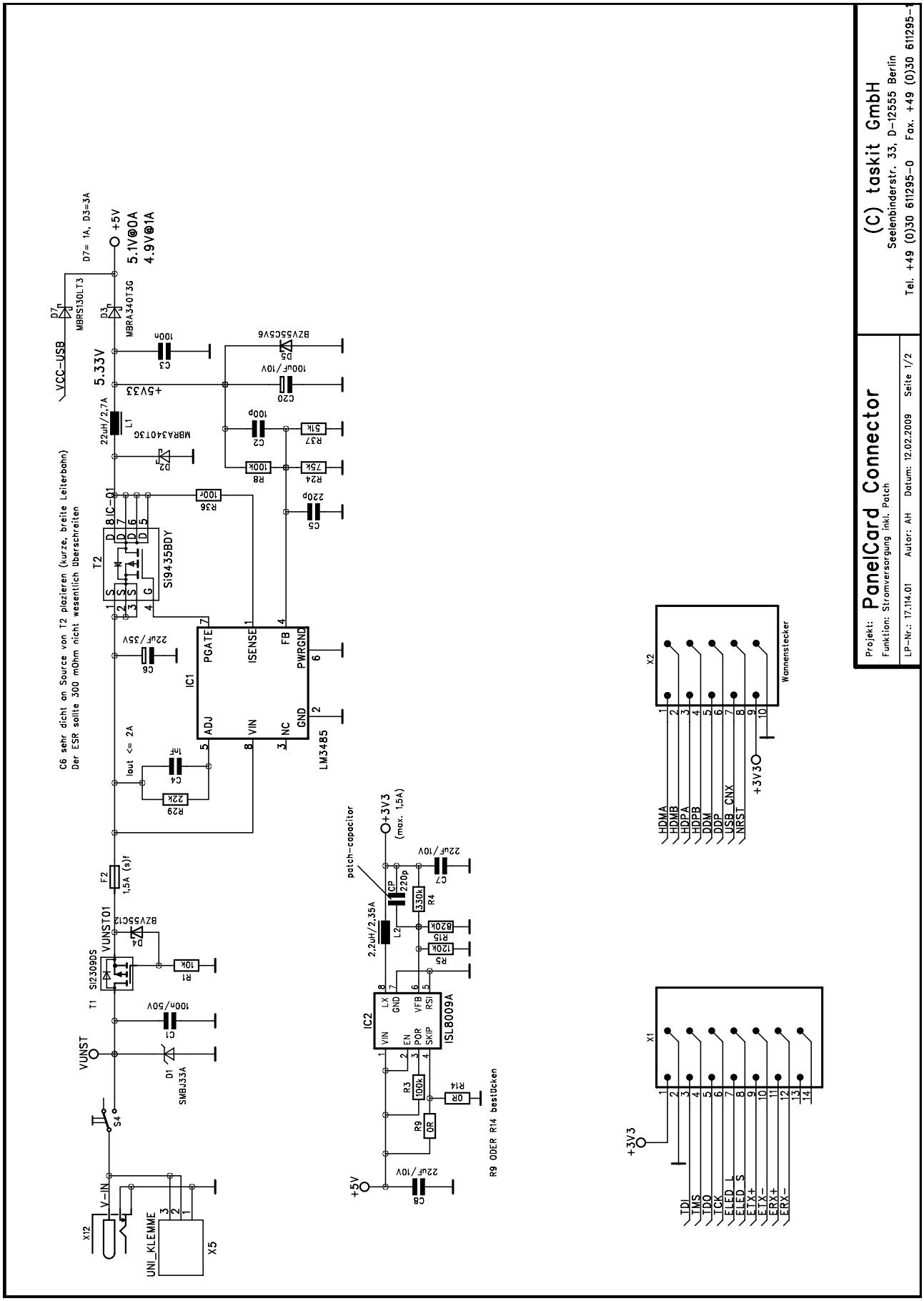

Figure 6.9. Panel-Card Connector Schematics Power Regulation/Connectors

Appendix A. Peripheral Color Codes

This table matches the color used to identify various peripherals in tables.

Power Supply/Ground
USART
Debug UART
TWI (I^2C-Bus)
SD-Card/MMC
SPI
USB Host
USB Device
Reserved
Synhcronous Serial Controller (SSC)
JTAG
Control
Ethernet
Genral Purpose I/O Port
Programmable Clock Output
Analog-to-digital Converter
Timer Counter
Image Sensor Interface
LCD/TFT Controller Interface
Embedded Trace Macrocell
Static Memory Controller
Compact Flash Interface
Pulse Width Modulator
Touch Controller
Can Controller
AC97 Sound Interface
Encryption Device
Soft Modem
True Random Generator

Appendix B. Peripheral Identifiers

ID	Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSIRQ	System Interrupt	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	-	Reserved	
6	US0	USART 0	
7	US1	USART 1	
8	US2	USART 2	
9	MCI	Multimedia Card Interface	
10	UDP	USB Device Port	
11	TWI	Two-Wire Interface	
12	SPI0	Serial Peripheral Interface 0	
13	SPI1	Serial Peripheral Interface 1	
14	SSC0	Synchronous Serial Controller 0	
15	SSC1	Synchronous Serial Controller 1	
16	SSC2	Synchronous Serial Controller 2	
17	TC0	Timer/Counter 0	
18	TC1	Timer/Counter 1	
19	TC2	Timer/Counter 2	
20	UHP	USB Host Port	
21	LCDC	LCD Controller	
22 - 28	-	Reserved	
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1
31	AIC	Advanced Interrupt Controller	IRQ2

Table B.1. Peripheral Identifiers

Appendix C. Address Map (Physical Address Space)

After the execution of the remap command the 4 GB physical address space is separated as shown in the following table. Accessing these addresses directly is only possible if the MMU (memory management unit) is deactivated. As soon as the MMU is activated the visible address space is changed completely. If absolute memory addresses should be accessed within an application, the corresponding address space has first to be mapped to the virtual address space using mmap or ioremap under Linux.

Address (Hex)	Mnemonic	Function
00 0000	Boot Memory	Flash (NCS0) or internal ROM or internal SRAM
10 0000	ITCM	Instruction TCM (Tightly Coupled Memory) Internal SRAM A: 0, 16, 32 or 64 kB
20 0000	DTCM	Data TCM (Tightly Coupled Memory) Internal SRAM B: 0, 16, 32 or 64 kB
30 0000	SRAM	Internal SRAM C SRAM A + SRAM B + SRAM C = 160 kB
40 0000	ROM	Internal ROM 32 kByte
50 0000	UHP	USB Host Port
60 0000	LCD	LCD Controller
1000 0000	EBI NCS0	Chip Select 0: Flash Memory #1, up to 128 MB
2000 0000	EBI NCS1	Chip Select 1: SDRAM, up to 64 MB
3000 0000	EBI NCS2	Chip Select 2: Ethernet Controller
4000 0000	EBI NCS3	Chip Select 3: Flash Memory #2, up to 128 MB
FFFA 0000	TC0, TC1, TC2	3 Timer Counter, 16-Bit
FFFA 4000	UDP	USB Device Port
FFFA 8000	MCI	Multimedia Card / SD-Card Interface
FFFA C000	TWI	Two Wire Interface (I²C)
FFFB 0000	USART0	Synchronous or Asynchronous Serial Port #0
FFFB 4000	USART1	Synchronous or Asynchronous Serial Port #1
FFFB 8000	USART2	Synchronous or Asynchronous Serial Port #2
FFFB C000	SSC0	Serial Synchronous Controller (I²S) #0
FFFC 0000	SSC1	Serial Synchronous Controller (I²S) #1
FFFC 4000	SSC2	Serial Synchronous Controller (I²S) #2
FFFC 8000	SPI0	Serial Peripheral Interface #0
FFFC C000	SPI1	Serial Peripheral Interface #1
FFFF EA00	SDRAMC	SDRAM Controller
FFFF EC00	SMC	Static Memory Controller
FFFF EE00	MATRIX	Bus Matrix User Interface
FFFF F000	AIC	Advanced Interrupt Controller
FFFF F200	DBGU	Debug Unit, including UART
FFFF F400	PIOA	32 Bit Parallel I/O Controller A
FFFF F600	PIOB	32 Bit Parallel I/O Controller B
FFFF F800	PIOC	32 Bit Parallel I/O Controller C

Address (Hex)	Mnemonic	Function
FFFF FC00	PMC	Power Management Controller
FFFF FD00	RSTC	Reset Controller, Battery Powered
FFFF FD10	SHDWC	Shutdown Controller, Battery Powered
FFFF FD20	RTT	Real-time Timer 32 Bit, Battery Powered
FFFF FD30	PIT	Periodic Interval Timer 32 Bit
FFFF FD40	WDT	Watchdog Timer
FFFF FD50	GPBR	4 General Purpose Backup Registers, Battery Powered

Table C.1. Physical Address Space

Appendix D. Panel-Card Pin Assignment

1	VCC			DSR1		PA27	2
3	PA23		RI1	RXD1		PC13	4
5	PC12		TXD1	DTR1		PA28	6
7	PA12		RTS1	CTS1		PA13	8
9	PA29		DCD1	GND			10
11	PA9	PCK2	DRXD	DTXD	PCK3	PA10	12
13	PA1	SPI0MOSI	MCCDA	MCCK	SPI0CLK	PA2	14
15	PA0	SPI0MISO	MCDA0	MCDA1	SPI0CS1	PA4	16
17	PA5	SPI0CS2	MCDA2	MCDA3	SPI0CS3	PA6	18
19	VCC			GND			20
21		USB Host A-		USB Host B-			22
23		USB Host A+		USB Host B+			24
25		USB Device-		USB Device+			26
27	PC2	IRQ0	USBCNX	/RESET			28
29	VCC			GND			30
31	PA17	TF1		RF1		PA22	32
33	PA18	TK1		RK1		PA21	34
35	PA19	TD1		RD1		PA20	36
37		BMS		WKUP			38
39		SHDN		VBATT			40

Table D.1. Pin Assignment and Multiplexing X1

1	VCC			SCK2		PA14	2
3	PA11		SCK1	RXD2		PC15	4
5	PC14		TXD2	TXD0	PCK2	PC8	6
7	PA15		RTS2	CTS2		PA16	8
9	PC9	PCK3	RXD0	GND			10
11	PA7	PCK0	TWD	TWCK	PCK1	PA8	12
13	VCC			GND			14
15	PB30	SPI1MISO	IRQ1	PCK2	SPI1MOSI	PB31	16
17	PB29	SPI1CLK	IRQ2		SPI1CS1	PA24	18
19	PA25	SPI1CS2			SPI1CS3	PA26	20
21							22
23							24
25							26
27	VCC			GND			28
29		TDI		TMS			30
31		TDO		TCK			32
33		ELED_L		ELED_S			34
35		ETX+		ETX-			36
37		ERX+		ERX-			38
39		POE1		POE2			40

Table D.2. Pin Assignment and Multiplexing X2

Appendix E. Panel-Card Electrical Characteristics

Ambient temperature 25℃, unless otherwise indicated

Symbol	Description	Parameter	Min.	Typ.	Max	Unit
V_{CC}	Operating Voltage		3.0	3.3	3.6	V
V_{RES}	Reset Treshhold			2.9		V
T_{RES}	Duration of Reset Pulse		150		280	ms
V_{IH}	High-Level Input Voltage	3.3V	2.0		V_{CC} + 0.3	V
V_{IL}	Low-Level Input Voltage	3.3V	-0.3		0.8	V
P	Normal Operation	ET035005DM6		1160		mW
		ET057011DHU		2330		mW
		ET057009DHU		3010		mW
	Normal Operation, LCD off	ET035005DM6		635		mW
		ET057011DHU		530		mW
		ET057009DHU		530		mW
	Full Load	ET035005DM6		1355		mW
		ET057011DHU		2430		mW
		ET057009DHU		3100		mW
	Power-Down	ET035005DM6		158		mW
		ET057011DHU		110		mW
		ET057009DHU		110		mW
V_{BATT}	Battery Voltage		2.0	3.0	V_{CC}	V
I_{BATT}	Battery Current	Ambient temp. = 25℃		5		µA
		Ambient temp. = 70℃			17	µA
		Ambient temp. = 85℃			22	µA

Table E.1. Electrical Characteristics

Appendix F. Panel-Card Clock Characteristics

Symbol	Description	Parameter	Dependency	Tolerance	Typical Value	Unit
MAINCK	Main Oscillator frequency				18.432	MHz
SLCK	Slow Clock				32.768	KHz
PLLACK	PLLA Clock		MAINCK		199.987	MHz
PCK	Processor Clock		PLLACK		199.987	MHz
MCK	Master Clock		PCK		99.994	MHz
SDCK	SDRAM Clock		MCK		99.994	MHz
BCK	Baudrate Clock		MCK	1.5%	6.250 (max)	MHz
PLLBCK	PLLB Clock		MAINCK		96.110	MHz
USBCK	USB Clock		PLLBCK	0.25%	48.005	MHz
LCDCK	LCD Dot Clock	ET035005DM6	MCK		6.250	MHz
		ET057011DHU	MCK		6.250	MHz
		ET057009DHU	MCK		24.999	MHz

Table F.1. Clock Characteristics

Appendix G. Panel-Card Environmental Ratings

Symbol	Description	Parameter	Operating		Storage		Unit
			Min.	Max.	Min.	Max.	
T_A	Ambient temperature	ET035005DM6	0	70	-30	80	℃
		ET057011DHU	0	60	-20	70	℃
		ET057009DHU	0	60	-20	70	℃
	Relative Humidity	no condensation		90		90	%RH
	Absolute Humidity		<= Humidity@T_A = 60℃, 90%RH				
	Corrosive Gas		not admissible				

Table G.1. Environmental Ratings

Appendix H. Panel-Card Dimensions

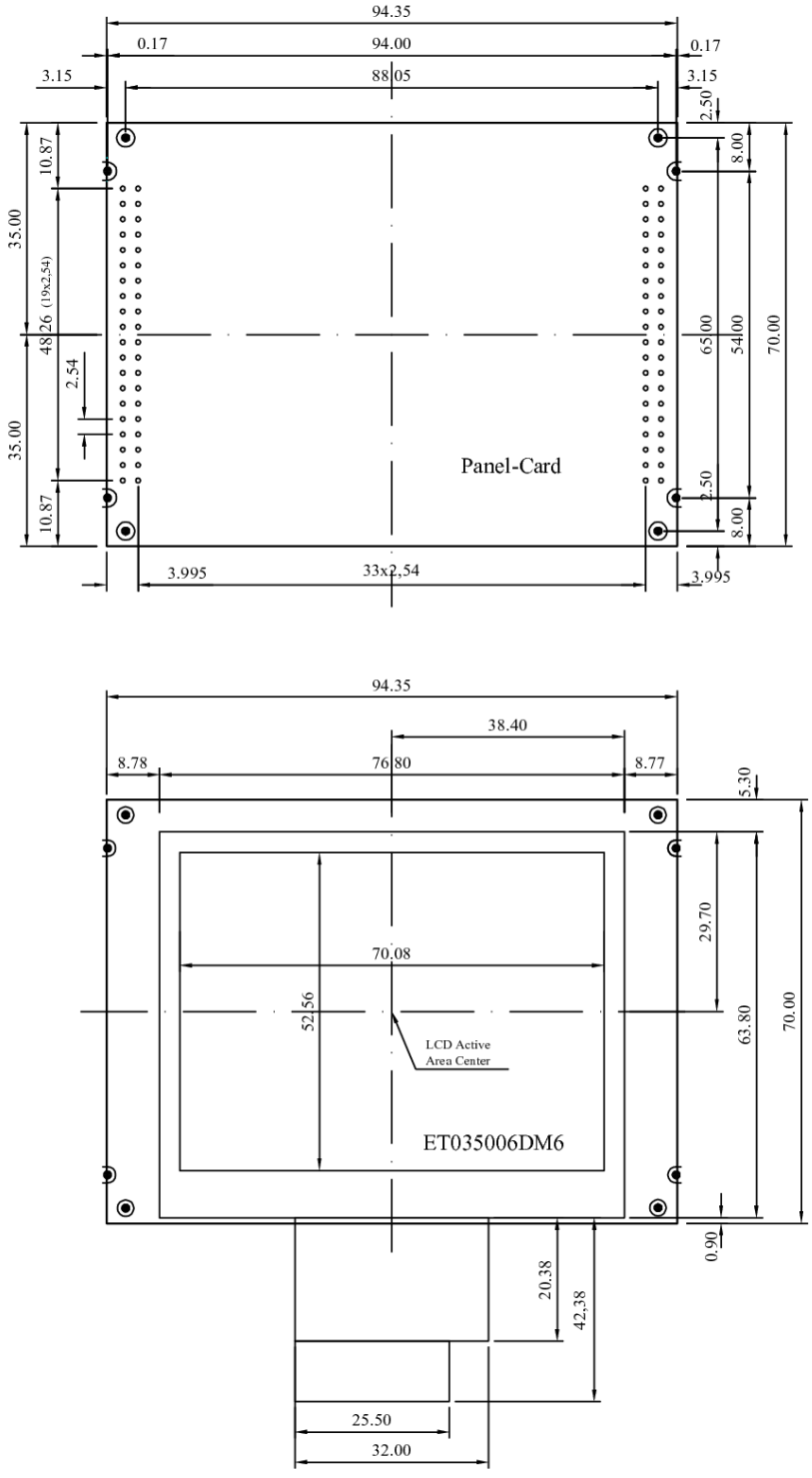

Figure H.1. Panel-Card 35 Dimensions

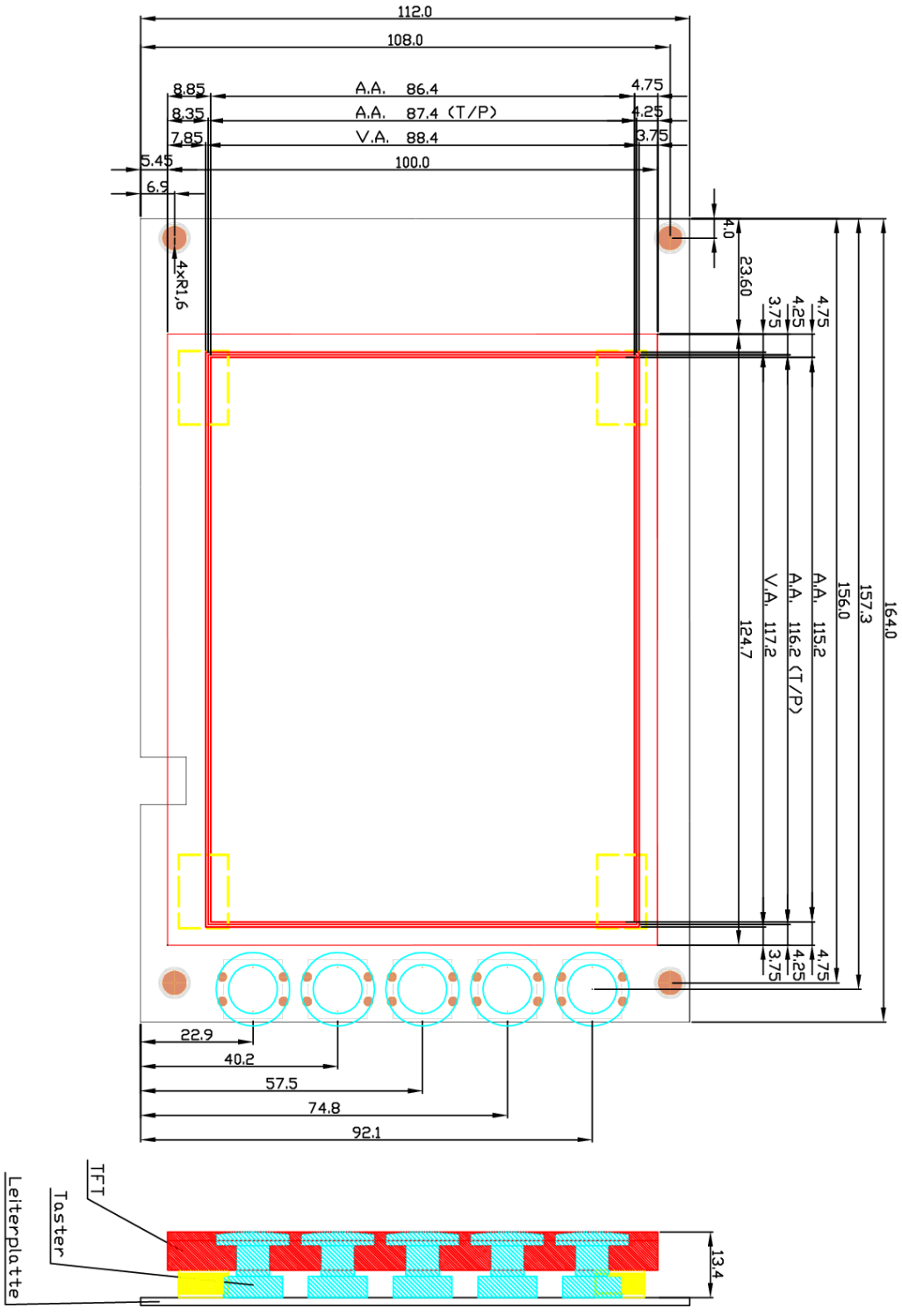

Figure H.2. Panel-Card 57 Dimensions

Appendix I. Desk70 Dimensions and Design

Figure I.1. Desk70 Outline

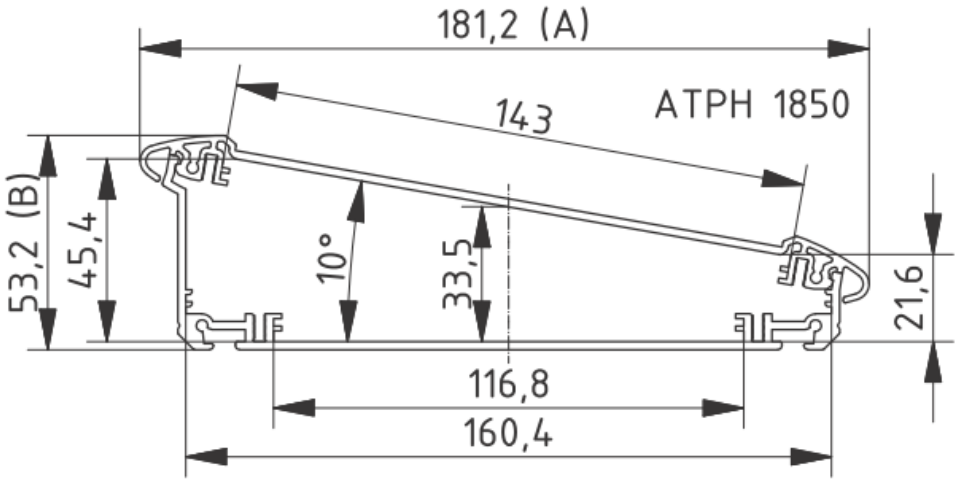

Figure I.2. Desk70 Dimensions

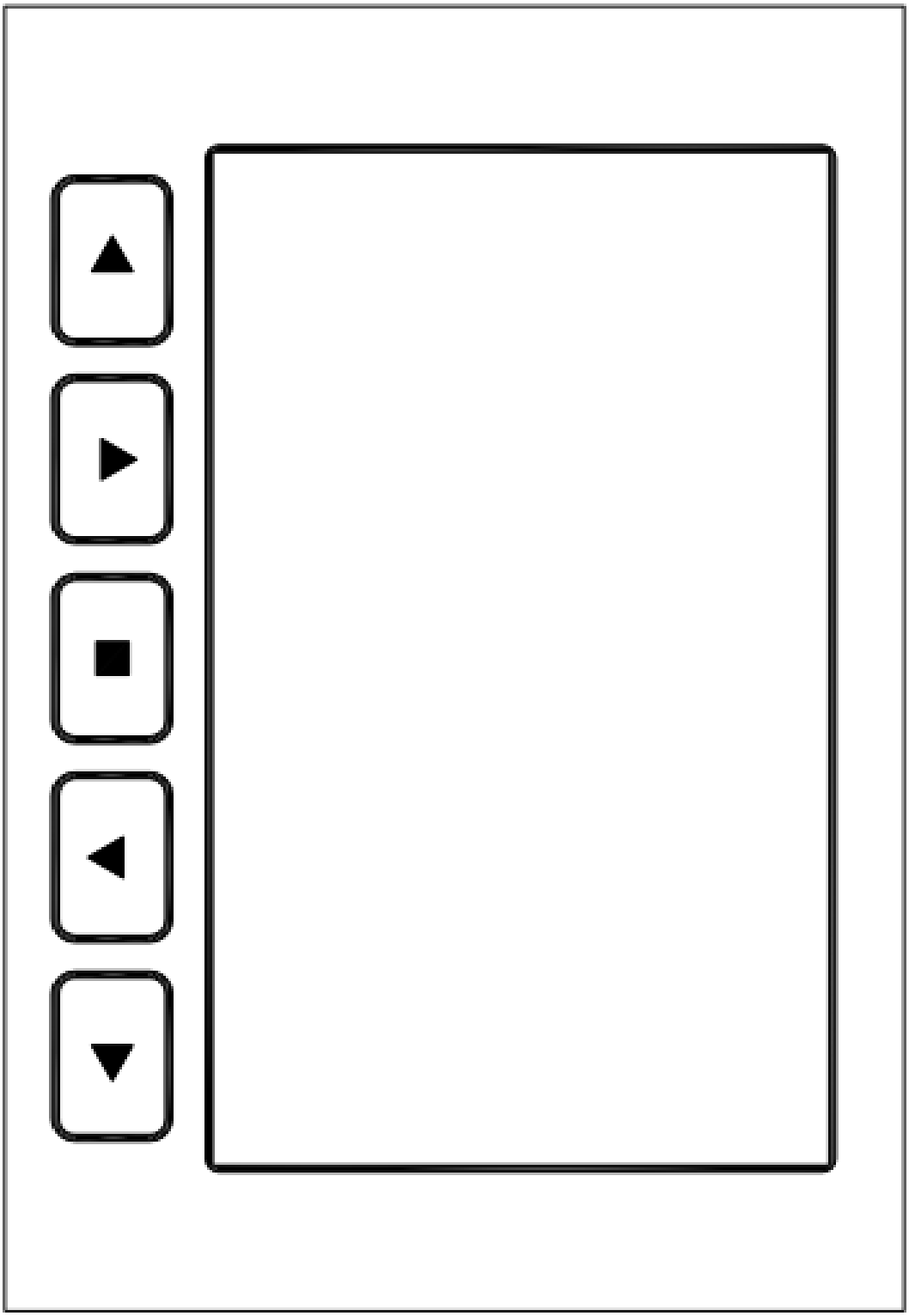

Figure I.3. Desk70 Front